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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,700	07/29/2004	Casey J. Grant	BUR920040052US1	4290

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EXAMINER	
MALSAWMA, LALRINFAMKIM HMAR	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 08/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,700	GRANT ET AL.	
	Examiner	Art Unit	
	Lex Malsawma	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) *23-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22 and 30-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2004 and 22 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 22, 2006 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1, 2, 4, 5, 10, 11, 12, 13, 15, 16, 21, 22 and 30-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Koze** (4,687,682) in view of and Kiyosumi et al. (4,603,059; hereinafter, "**Kiyosumi**").

Regarding claims 1, 2, 5 and 36:

Koze discloses a method of fabricating semiconductor wafer 100 (Fig. 1), comprising:

providing a plurality of semiconductor wafers 100, wherein the plurality of wafers comprises a first semiconductor wafer and a second semiconductor wafer, and wherein the first semiconductor wafer is located adjacent to the second semiconductor wafer (note in Fig. 1, any of wafers 100 could be chosen as the first and second wafers);

choosing a material (silicon dioxide and/or silicon nitride) and forming a substructure comprising the material placed between a topside of the first semiconductor wafer and a backside of a portion of the second semiconductor wafer (note Col. 1, lines 44-63, i.e., a capping layer comprising silicon dioxide and silicon nitride is formed on the backside of the wafers prior to epitaxially growing a layer on the front sides of the wafers; furthermore, note that a gas would occupy an entire space between said topside of the first semiconductor wafer and a first side of said MATERIAL at least during the epitaxial growth process, i.e., Koze discloses in Col. 3, lines 55-57, the wafers "are then ready for the epitaxial growth process according to procedures known in the art", wherein during the epitaxial growth process, a gas would occupy an entire space between the topside of the first wafer and the first side of the "protective" material, which had been formed on the backside of each wafer prior to the epitaxial growth process, note Col. 1, lines 25-49, wherein Koze describes a function for "the protective material" during an epitaxial growth process, i.e., during the epitaxial growth process performed after each of the wafer has

been provided with a substructure on its backside, a gas will occupy an entire space between the topside/frontside of the first wafer and the first side of the "protective" material formed on the backside of the second wafer); and

placing the plurality of wafers into an apparatus for processing (i.e., for forming an epitaxial layer at an elevated temperature, note Col. 1, lines 25-31 and Col. 3, lines 55-57), wherein the apparatus comprises an elevated temperature (note that an apparatus operated at an elevated temperature could be referred to as a furnace).

Koze **lacks** specifically providing a relationship between a plurality of values for an electrical characteristic and a plurality of materials; and the processing at the elevated temperature resulting in a value for the first semiconductor wafer of the electrical characteristic that corresponds to said material in the relationship. Although Koze does not specifically recite a relationship as in the current claims, one of ordinary skill in the art would have readily recognized that the material(s) specified by Koze (silicon dioxide and silicon nitride) would inherently have a relationship between an electrical characteristic and the material(s) even when the elevated temperature for epitaxial growth is combined with said material. Kiyosumi is **cited to show** at least one relationship between a plurality of values for electrical characteristic and a plurality of materials that one could readily recite/specify with respect to the materials used by Koze. In Fig. 4, Kiyosumi shows a relationship between an electrical characteristic and a material such as silicon dioxide and/or silicon nitride.

It would have been obvious to one of ordinary skill in the art to modify Koze by specifying a relationship (as currently claimed) because Kiyosumi shows that the material(s) specified by Koze would obviously (if not inherently) have some kind of relationship between

values for an electrical characteristic and the material(s). Furthermore, Koze discloses that the capping material(s) remains throughout (and after) the elevated-temperature process (i.e., epitaxial process, note Col. 1, lines 60-63); accordingly, it could readily be said that the elevated-temperature results in a value for the first wafer of the electrical characteristic that corresponds to the material in the relationship, i.e., because the capping material remains after the elevated-temperature process, a value of the electrical characteristic will correspond to the capping material in the relationship, and because each wafer has the "capping" material formed thereon, the wafers (including the first wafer) have a value of the electrical characteristic that corresponds to the "capping" material in the relationship. *Specifically regarding claim 36:* the material, i.e., the protective material formed on the backsides of each wafer will have a second side that is exposed to the gas during the epitaxial growth process. In other words, the second side of the material would be the side surface of material, and this side surface would be exposed to the gas during the epitaxial growth process.

Regarding claim 4:

Koze discloses at least five wafers 100 on each boat 101 (note Fig. 1), wherein each wafer will have the capping material formed on its backside. I would have been obvious to one of ordinary skill in the art modify Koze (in view of Kiyosumi) by specifying that a monitor wafer comprising the material is placed between the second and first wafers because any of the wafers 100 (shown in Fig. 1) could be referred to as the first wafer, the second wafer and a monitor wafer. In other words, there is nothing in Koze (or Kiyosumi) to prevent one from referring to one of the wafers 100 as a monitor wafer, which is sandwiched between the first and second wafers.

Regarding claims 10 and 11:

Kiyosumi shows (in Fig. 4) the relationship is a graphical relationship; and given Kiyosumi, one of ordinary skill in the art could have easily chosen discrete points and expressed the relationship in a tabular form. Therefore, these claims are deemed obvious over the cited references.

Regarding claims 12, 13, 15, 16, 21 and 22:

These claims are similar to, or essentially the same as, claims 1, 2, 4, 5, 7 and 9-11 **except** that they include limitations directed to features in accordance with third and fourth semiconductor wafers. In general, these claims are deemed obvious over the cited reference for reasons similar to those provided in detail above with respect to claims 1, 2, 4, 5, 7 and 9-11.

More specifically, with respect to claim 12, Koze discloses (in Fig. 1) at least five boats 101, each of which holds at least 5 semiconductor wafers 100; accordingly, Koze discloses at least a third and fourth semiconductor wafer. Koze discloses the "capping" material comprises silicon dioxide and silicon nitride (Col. 1, lines 44-63 and Col. 3, lines 25-28 and 38-40), wherein each of the wafers comprises the capping material; therefore, the silicon dioxide layer (or the silicon nitride layer) could readily serve as the first material of the first substructure (of the current claims) and a combination of the silicon dioxide and the silicon nitride layer could readily serve as the second material of the second substructure (of the current claims). Furthermore, Koze discloses the capping material(s) remains throughout (and after) the elevated-temperature process (i.e., the epitaxial process, note Col. 1, lines 60-63); accordingly, the elevated temperature process would result in (1) a first value of the electrical characteristic the corresponds to the first material (silicon dioxide or silicon nitride) in the relationship and (2) a

second value for the 3rd and 4th wafers of the characteristic that corresponds to the second material (a combination of silicon dioxide and silicon nitride), wherein the first value is not the same as the second value, i.e., note that Kiyosumi shows (in Fig. 4) an electrical characteristic (e.g., leakage current) for silicon dioxide is not the same as that for a combination of silicon dioxide and silicon nitride.

With respect to claim 15, a "center" wafer 100 (in Koze, Fig. 1) within one boat 101 could be chosen as the first monitor wafer and a "center" wafer 100 within another boat 101 could be chosen as the second monitor wafer, wherein the two wafers sandwiching the "center" wafer in the first boat would be the first and second wafers and the two wafers sandwiching the "center" wafer in the other boat would be the third and fourth wafers.

With respect to claims 13, 16, 21 and 22, the reasoning provided above for claim 2, 5, 10 and 11 should be sufficient without further explanation.

Regarding claims 30-35:

Koze discloses (in Col. 3, lines 1-7) each of the plurality of wafers has an active face, i.e., the frontside of each wafer is for active components. The active face of each wafer inherently has a value for an electrical characteristic such a polysilicon sheet resistance (even if the value is zero); therefore, these claims are deemed obvious over the cited references.

5. Claims 3 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Koze** (in view of **Kiyosumi**) as applied to claims 1 and 12 above, and further in view of Moslehi et al. (5,296,385; hereinafter "**Moslehi**").

Regarding claim 3:

Koze (in view of Kiyosumi) **lacks** removing at least one layer of a first material from the backside to expose the material. Moslehi **teaches** a process similar to that of Koze, wherein Moslehi conditions semiconductor wafers for subsequent processing (note Moslehi, Figs. 1-5 and Col. 1, line 66 to Col. 2, line 36). Moslehi conditions the wafers by forming a "capping" material 8/10 (oxide/nitride) on the backside of the wafers, followed by forming a photoresist 12 on the "capping" material such that the front side of the wafers can be conditioned, and then removing the photoresist 12 from the "capping" material 8/10. Moslehi discloses a plurality of advantages for conditioning wafers in this manner (note Col. 4, beginning from line 40), wherein the advantages include providing constant backside layers yielding a non-varying wafer backside structure.

It would have been obvious to one of ordinary skill in the art to modify Koze (in view of Kiyosumi) by incorporating at least one layer of material (e.g., a photoresist) on the backside "capping" material as taught by Moslehi because such a modification could provide significant advantages such as constant backside layers yielding a non-varying wafer backside structure. Note that Koze (in view of Kiyosumi) modified as taught by Moslehi would result in removing the at least one layer (i.e., the photoresist) to expose the "capping" material on each wafer.

Regarding claim 14:

This claim is generally deemed obvious over the cited references for reasons similar to those provided above with respect to claim 3. Furthermore, note that the first material (with respect to this claim) would be the silicon nitride layer and the second material would be the silicon-dioxide/silicon-nitride combination (note above, *Regarding claims 12, 13, 15, 16, 21 and*

22), wherein a value for the electrical characteristic corresponding to the first material would not be the same value as that for the second material, e.g., note Kiyosumi, Fig. 4, wherein an electrical characteristic of Si_3N_4 would not be the same as that for SiO_2/Si_3N_4 because an electrical characteristic for $SiO_2/Si_3N_4/SiO_2$ is not the same as that for SiO_2/Si_3N_4, i.e., if the value for Si_3N_4 were to be the same as that for SiO_2/Si_3N_4, then the value for SiO_2/Si_3N_4 would be equal to that for "SiO_2/Si_3N_4"/SiO_2 (where "SiO_2/Si_3N_4" would be equal to "Si_3N_4"), however, this is not the case; accordingly, an electrical characteristic of Si_3N_4 would not be the same as that for SiO_2/Si_3N_4.

6. Claims 6-9 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Koze** (in view of **Kiyosumi**) as applied to claims 5 and 16 above, and further in view of **Sugino** (5,121,705).

Regarding claims 6 and 8:

Koze (in view of Kiyosumi) **lacks** specifying any particular type of apparatus/furnace used to process the wafers after "capping" the backsides of each wafer. Sugino is **cited to show** it was very well known in the art to utilize apparatuses such as an LPCVD apparatus to perform epitaxial growth (note Sugino, Col. 8, lines 43-49), i.e., to perform a process similar to that disclosed by Koze. Note that Koze also discloses using a furnace for growing an oxide (Col. 1, lines 51-53). It is further noted that any LPCVD apparatus/furnace could be readily referred to as a polysilicon LPCVD furnace because polysilicon is just one of numerous materials typically formed with an LPCVD furnace, and the same applies for an oxidation furnace that is specifically referred to as a gate oxidation furnace.

It would have been obvious to one of ordinary skill in the art to modify Koze (in view of Kiyosumi) by specifically reciting that a polysilicon LPCVD furnace or a gate oxidation furnace is utilized because Sugino shows that a process similar to that performed by Koze is readily performed using an LPCVD furnace and Koze already suggests using an oxidation furnace when forming the "capping" material, accordingly, an oxidation furnace would already be available if a gate oxidation process is specifically chosen for the processing step recited in claim 1. Therefore, these claims are deemed obvious over the cited references primarily because apparatuses that could be specifically referenced as polysilicon LPCVD or gate oxidation furnaces would be provided by Koze (in view of Kiyosumi and Sugino).

Regarding claims 7 and 9:

Koze (in view of Kiyosumi) does not specifically disclose the electrical characteristic is polysilicon sheet resistance or a gate oxide thickness; however, there is apparently no criticality for the recited electrical characteristic. In other words, the "capping" material disclosed by Koze would have a polysilicon sheet resistance of some value (even if the value is zero) and a thickness of some value, and whether one specifically refers to the electrical characteristic of Koze's "capping" material in terms of polysilicon sheet resistance, gate oxide thickness or leakage current (as shown by Kiyosumi in Fig. 4) would not be critical because the important aspect of the method would reside in the particular material chosen for the "capping" material. In other words, once a material is chosen/utilized (as in Koze) for the "capping" material, one of ordinary skill in the art could easily refer to the electrical characteristics of the "capping" material in a variety of different ways including those currently recited or as shown by Kiyosumi (i.e., leakage current).

Regarding claims 17-20:

These claims are similar to claims 6-9, accordingly, they are deemed obvious over the cited references with reasoning similar to those applied above to claims 6-9.

Status of the Claims

7. Claims 1-22 and 30-36 stand rejected under 35 USC § 103.

8. Clams 23-29 remain withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention.

Remarks

9. Applicants' remarks have been carefully reviewed and considered, however, no comments/arguments were provided with respect to the applied references and/or how the current amendments clearly define subject matter that would patentably distinguish over the applied references. In general, the amendments to the claims are not considered to patentably distinguish over the cited references primarily because "the gas" specified in claims 1 and 12 is required to occupy an entire space between the topside of the first wafer and a first side of the material. In other words, the material must already be formed (or exist) in order for the gas to occupy an entire space as currently recited in claims 1 and 12; accordingly, Koze discloses this feature because Koze's epitaxial growth process is performed after the material is formed on the backside of each wafer, wherein Koze utilizes well known processes for the epitaxial growth and well-known processes would include processing a plurality of wafers simultaneously such that the topside of the first wafer would be spaced from the "protective" material, which is formed on the backside of the second wafer. Lastly, it is noted the claim language does not require "the placing step" recited in claims 1 and 12 to be a separate/distinct processing step that follows "the

substructure forming step", i.e., once the substructure ("said material") is formed on the backside of each wafer, Koze discloses performing an epitaxial growth process by well known processes, wherein during the epitaxial growth process, a gas would occupy an entire space as currently claimed in claims 1 and 12.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lex Malsawma whose telephone number is 571-272-1903. The examiner can normally be reached on Mon. - Thur. (4-12 hours between 5:30AM and 10 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Lex Malsawma
August 7, 2006